PRIORITY

Applicants appreciate the Examiner's acknowledgement of the claim for priority and safe receipt of the certified priority document filed in a parent application.

35 U.S.C. §112

The claims have been amended to overcome the Examiner's rejections.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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Date: February 19, 2003

MARKED UP VERSION OF REWRITTEN CLAIMS

37. (Amended) A semiconductor memory apparatus comprising:

a plurality of semiconductor memory devices;

[a] each of said semiconductor memory devices comprising a source region and a drain region, a semiconductor current path connected between the source and the drain regions, a plurality of small [memory] charge storage nodes surrounded [covered] by an insulator which acts as a potential barrier [over] for the [periphery of the memory] charge storage nodes, wherein said charge storage node is located between said control gate and said current path [a control electrode controlling a voltage of the current path and the memory nodes];

[a] wherein said plurality of [the] semiconductor memory devices [storing an] stores information by a difference of an electron charge stored in each [memory] said charge storage node;

a plurality of control gates connected to each other between [the plural] a plurality of said semiconductor memory devices; and

wherein a voltage applied between the source and the drain region in the semiconductor memory device is different according to the difference in information to be written in a

writing operation for different information stored in each of said [in the] plurality of semiconductor memory device.

38. (Amended) The semiconductor memory [device] apparatus according to claim 37, wherein a large voltage among the voltage applied between the source and the drain regions in the semiconductor memory devices is over 3 V in the writing operation of the information.

39. (Amended) The semiconductor memory device according to claim 37, wherein a small voltage among the voltage applied between the source and the drain regions in the semiconductor memory devices is substantially 0 V in the writing operation of the information.

40. (Amended) The semiconductor memory device according to claim 37, wherein a positive/negative polarity of the voltage applied between the source and the drain regions in [the] a reading operation [for the] to read a stored information is opposite from a positive/negative polarity of the voltage applied between the source and the drain regions in the writing operation.

41. (Amended) The semiconductor memory device according to claim 37, wherein the source and drain regions and the current path is located on [the] an insulator film.